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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,539	04/15/2002	Anand S. Murthy	42390.P6624PCT	6105

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/831,539	Applicant(s) MURTHY ET AL.	
	Examiner Brook Kebede	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I, Claims 1-10, drawn to Semiconductor Device, classified in class 257, subclass 213+.

Group II, Claims 11-30, drawn to Method of Fabricating Semiconductor Device, classified in class 438, subclass 300.

2. The inventions are distinct, each from the other because of the following reasons:

3. Inventions Group II and Group I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the device of Group I can be manufactured by forming a dummy gate and a gate dielectric and sidewall spacers pattern and forming recess into the substrate under the dummy gate and filling the recess with a material having a second conductivity and masking the filled recess and removing the dummy gate to form a void and filling the void with material of first conductivity.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mr. Michael A. Bernadicou on September 5, 2002 a provisional election was made with traverse to prosecute the invention of Group II, claims 11-30. Affirmation of this election must be made by applicant in replying to this Office action.

6. Claims 1-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 11-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Murthy et al. (WO 00/30169).

Re claim 11, Murthy et al. disclose a method of making a junction, comprising: a) forming a patterned structure on a surface of a substrate, the substrate being of a first conductivity type; b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the patterned structure, the recess having a surface; and c) selectively forming a layer of a first material having a second conductivity type in the recess (see Figs. 1-7 and Page 17-21).

Re claim 12, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation prior to selectively forming the layer of the first material, selectively forming a layer of a second material having the first conductivity type over the surface of the recess (see Figs. 1-7 and Page 17-21).

Re claim 13, as applied to claim 12 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon (see Figs. 1-7 and Page 17-21).

Re claim 14, as applied to claim 12 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon germanium, and the second material comprises doped silicon germanium (see Figs. 1-7 and Page 17-21).

Re claim 15, as applied to claim 14 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the second material has a thickness that is less than a thickness of the first material (see Figs. 1-7 and Page 17-21).

Re claim 16, as applied to claim 15 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the first material has a top surface that is above a plane defined by the surface of the substrate (see Figs. 1-7 and Page 17-21).

Re claim 17, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer (see Figs. 1-7 and Page 17-21).

Re claim 18, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation wherein etching passivates the surface of the recess (see Figs. 1-7 and Page 17-21).

Re claim 19, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation wherein etching comprises exposing the substrate to SF6 and He in an R-F plasma etching system (see Figs. 1-7 and Page 17-21).

Re claim 20, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation wherein forming the first material comprises epitaxially depositing a layer of crystalline material (see Figs. 1-7 and Page 17-21).

Re claim 21, as applied to claim 11 above, Murthy et al. disclose all the claimed limitations including the limitation wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprises epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material (see Figs. 1-7 and Page 17-21).

Re claim 22, Murthy et al. disclose a method of making a transistor, comprising: forming a dielectric on a first surface of a wafer; forming a conductive layer overlying the dielectric; patterning the conductive layer and dielectric so as to form a gate structure; forming recesses adjacent and partially subjacent the gate structure; and in a continuous operation, back filling the recesses with doped crystalline material; wherein back filling comprises forming crystalline material of at least a first conductivity type (see Figs. 1-7 and Page 17-21).

Re claim 23, as applied to claim 22 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 1-7 and Page 17-21).

Re claim 24, as applied to claim 22 above, Murthy et al. disclose all the claimed limitations including the limitation wherein back filling further comprises forming crystalline material of a second conductivity type (see Figs. 1-7 and Page 17-21).

Re claim 25, as applied to claim 22 above, Murthy et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 1-7 and Page 17-21).

Re claim 26, as applied to claim 25 above, Murthy et al. disclose all the claimed limitations including the limitation wherein back filling comprises a selective deposition (see Figs. 1-7 and Page 17-21).

Re claim 27, Murthy et al. disclose a method of fabricating a FET, comprising: forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type; forming first spacers along the sidewalls of the gate electrode; forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface; substantially filling the recess with a fist layer of doped crystalline material, the first layer having a second conductivity type (see Figs. 1-7 and Page 17-21).

Re claim 28, as applied to claim 27 above, Murthy et al. disclose all the claimed limitations including the limitation further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate (see Figs. 1-7 and Page 17-21).

Re claim 29, as applied to claim 27 above, Murthy et al. disclose all the claimed limitations including the limitation forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess (see Figs. 1-7 and Page 17-21).

Re claim 30, as applied to claim 29 above, Murthy et al. disclose all the claimed limitations including the limitation wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1. 1 cm, an RF power in the range of approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium (see Figs. 1-7 and Page 17-21).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Hwang et al. (US/5,620,912), Liang et al. (US/6,071,783) and Fulford, Jr. et al. (US/6,187,620) also disclose similar inventive subject matter.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
September 7, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800